What is claimed is:

1. An apparatus performing compaction of a set of test stimuli for a digital circuit, comprising:

a selection device selecting essential test stimuli from among subsets of the set of test stimuli, an essential test stimulus being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of test stimuli;

an elimination device eliminating redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset; and

an output device outputting a compacted set comprising the selected essential test stimuli.

2. The apparatus according to claim 1, wherein

said output device outputs a minimum-sized subset of the set of test stimuli, which covers faults detectable by the set of test stimuli without modifying test stimuli in the minimum-sized subset, as the compacted set.

3. The apparatus according to claim 1, wherein

said selection device hierarchically repeats the selection of essential test stimuli from among subsets

of remaining test stimuli after elimination of redundant test stimuli from the subsets, and said output device outputs the compacted set comprising the selected essential test stimuli.

4. The apparatus according to claim 1, wherein

said elimination device identifies a subset of test stimuli that optimally covers a given set of faults and eliminates one or more test stimuli other than the identified test stimuli as the redundant test stimuli.

5. The apparatus according to claim 1, further comprising

a storage device storing information of the set of test stimuli, information of faults which the set of test stimuli cover, and pointing information associating each test stimulus with the faults detectable by a corresponding test stimulus,

wherein said selection device and elimination device perform selection and elimination, respectively by referring to the information stored in said storage device.

6. The apparatus according to claim 5, further comprising

a simulation device performing a simulation on the digital circuit with the set of test stimuli to trace the faults which the set of test stimuli cover,

wherein said storage device stores counter information associated with each fault and indicating the number of test stimuli by which a corresponding fault is detectable, said simulation device increments the counter information when the corresponding fault is traced during the simulation, and said selection device selects a test stimulus which covers a fault with counter information of one as an essential test stimulus.

7. The apparatus according to claim 1, wherein

the apparatus performs compaction of the set of test stimuli by which faults of a stuck-at fault model are detectable.

8. The apparatus according to claim 1, wherein

the apparatus performs compaction of the set of test stimuli by which faults of a delay fault model are detectable.

9. The apparatus according to claim 1, wherein

the apparatus performs compaction of the set of test stimuli by regarding a sequence of initializing,

sensitizing and propagation subsequences as a single test stimulus.

10. A computer readable recording medium storing a program for a computer that performs compaction of a set of test stimuli for a digital circuit, the program causes the computer to perform:

selecting essential test stimuli from among subsets of the set of test stimuli, an essential test stimulus being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of test stimuli;

eliminating redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset; and

outputting a compacted set comprising the selected essential test stimuli.

11. A propagation signal propagating a program to a computer that performs compaction of a set of test stimuli for a digital circuit, the program causes the computer to perform:

selecting essential test stimuli from among subsets of the set of test stimuli, an essential test stimulus being a test stimulus that detects at least

one fault, which is detectable by no other test stimulus in one of the subsets of test stimuli;

eliminating redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset; and

outputting a compacted set comprising the selected essential test stimuli.

12. A method for compaction of a set of test stimuli for a digital circuit, comprising:

selecting essential test stimuli from among subsets of the set of test stimuli, an essential test stimulus being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of test stimuli;

eliminating redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset; and

outputting a compacted set comprising the selected essential test stimuli.

13. An apparatus performing compaction of a set of test stimuli for a digital circuit, comprising:

selection means for selecting essential test stimuli from among subsets of the set of test stimuli,

an essential test stimulus being a test stimulus that detects at least one fault, which is detectable by no other test stimulus in one of the subsets of test stimuli;

elimination means for eliminating redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset; and

output means for outputting a compacted set comprising the selected essential test stimuli.